I claim:

1. A configuration for calibrating an interface, with a plurality of parallel transfer channels for transmission of a number of parallel data signals and, optionally, command signals between associated outer connections and associated circuit nodes in an electronic assembly, and with at least one synchronization signal connection for a synchronization signal determining a time base for the parallel-transmitted signals, comprising:

individually controllable delay devices respectively contained in selected transfer channels for setting a time delay for the signal transmission in the respective transfer channel as a function of a delay control signal;

a control device connected in the interface and including a sensing means for sensing, in each selected transfer channel, an actual value of a relative phase of the respective data signal with respect to an associated, accompanying synchronization signal, and means for producing the delay control signal in dependence on a respectively sensed actual value for controlling each of said delay devices in order to match the actual value to a predetermined, common setpoint value.

2. The configuration according to claim 1, wherein each said controllable delay device is formed by a variable delay element, inserted into a signal path carrying the signal to be transmitted, of the respective transfer channel.

3. The configuration according to claim 1, which comprises a latch circuit connected to pass the signal to be transmitted through a respective transfer channel, and wherein each said controllable delay device is formed by a variable delay element in a latch signal line connected to said latch circuit.

4. The configuration according to claim 1, which comprises a separate phase detector contained in each selected transfer channel, said phase detectors each having a signal input connected for receiving the signal delayed by a respectively associated said controllable delay device, a reference input connected for receiving the associated synchronization signal, and an output the connected to a delay control input of the respective said delay device and carrying a sense signal indicating a magnitude and a direction of a time shift between flanks of the input signals present at said two inputs.

5. The configuration according to claim 1, wherein the selected transfer channels are transfer channels transmitting received signals from the outer connections to the assembly.

6. The configuration according to claim 5, wherein the selected transfer channels also include transfer channels for transmitting signals from the assembly to the outer connections.

7. The configuration according to claim 1, wherein said control device further comprises:

a memory device for temporarily storing the delay control signals being produced;

a monitoring device for monitoring the signals to be transmitted via the selected transfer channels and for producing an activation command when the signals contain transitions that can be uniquely associated with the time base; and

a switching device for applying a temporarily stored delay control signal to the relevant delay device only when said monitoring device produces an activation command.

8. The configuration according to claim 7, wherein said monitoring device is configured to produce the activation command for the binary data signals to be transmitted, when two binary transitions occur in the signals within a time

window greater than one bit period and smaller than two bit periods.

9. A method of calibrating an interface having a plurality of parallel transfer channels, the method which comprises:

temporarily switching on the control device according to claim 1, prior to a start of user operation of the interface or in pauses during user operation; and

causing a source supplying the signals to be transmitted via the selected transfer channels, while the control device is in the switched-on state, to produce the signals in each case as a pattern signal with signal transitions that can be uniquely associated with the time base.

10. The method according to claim 9, which comprises producing a periodic binary sequence as the pattern signal.

11. The method according to claim 10, wherein the periodic binary sequence is a binary sequence alternating bit-by-bit.

12. The method according to claim 9, which comprises producing a pseudo-random sequence of binary values as the pattern signal.

13. A method of calibrating an interface, which comprises providing a configuration according to claim 1, and at least temporarily activating the control device during user operation of the interface.

14. The method according to claim 13, which comprises keeping the control device activated for examples of the selected transfer channels during user operation of the interface, but applying any delay control signals produced in that case to the relevant delay device only when transitions occur in the signal to be transmitted via the relevant transfer channel that can be uniquely associated with the time base.

15. A method of calibrating an interface, which comprises providing a configuration according to claim 7, and maintaining the configuration in operation during a user operation of the interface.